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Yang et al.

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(54) **SEMICONDUCTOR ARRANGEMENT AND FORMATION THEREOF**

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(51) **Int. Cl.**

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H01L 21/768	(2006.01)
H01L 29/66	(2006.01)
H01L 29/49	(2006.01)
H01L 29/78	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/76897*** (2013.01); ***H01L 29/4958*** (2013.01); ***H01L 29/6656*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/78*** (2013.01); *H01L 29/66575* (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/336; H01L 21/76897; H01L 29/4958; H01L 29/66545

USPC 257/E21.444; 438/183

See application file for complete search history.

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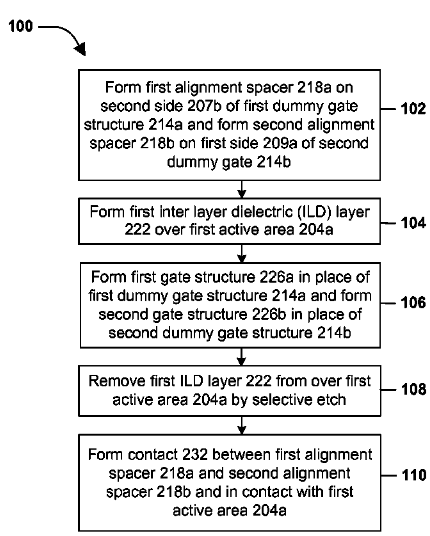
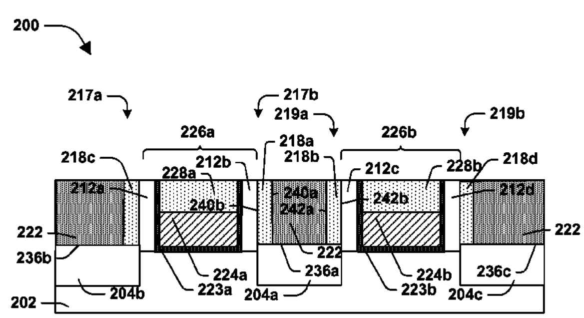
(57) **ABSTRACT**

A semiconductor arrangement and method of formation are provided. The semiconductor arrangement comprises a conductive contact in contact with a substantially planar first top surface of a first active area, the contact between and in contact with a first alignment spacer and a second alignment spacer both having substantially vertical outer surfaces. The contact formed between the first alignment spacer and the second alignment spacer has a more desired contact shape then a contact formed between alignment spacers that do not have substantially vertical outer surfaces. The substantially planar surface of the first active area is indicative of a substantially undamaged structure of the first active area as compared to an active area that is not substantially planar. The substantially undamaged first active area has a greater contact area for the contact and a lower contact resistance as compared to a damaged first active area.

20 Claims, 8 Drawing Sheets





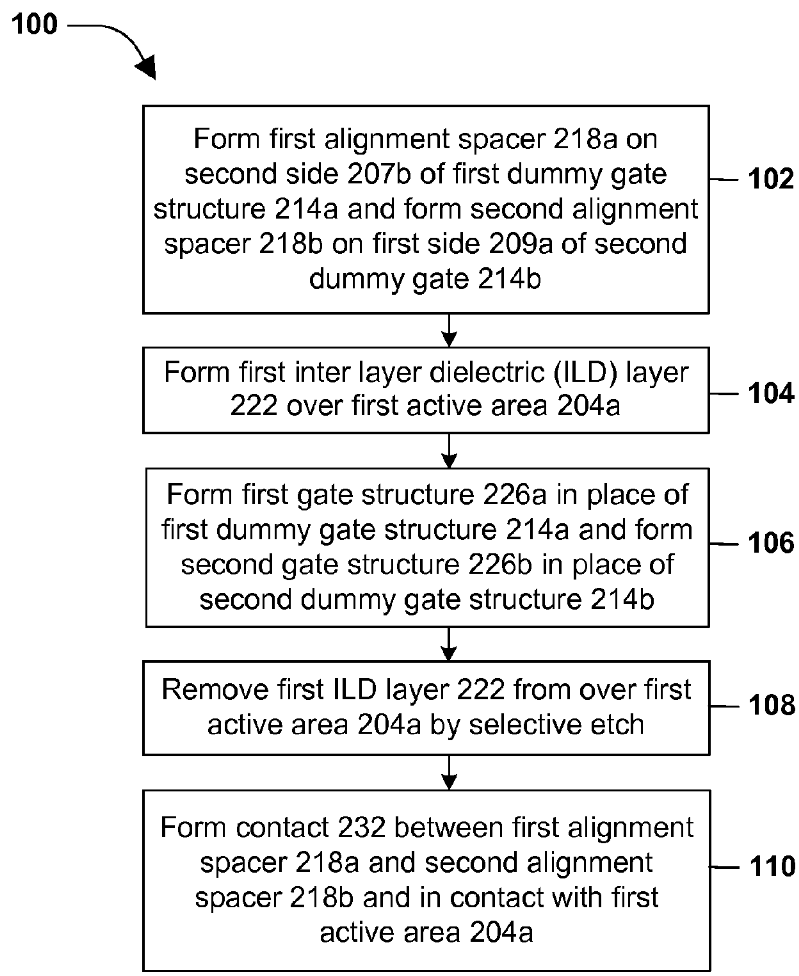
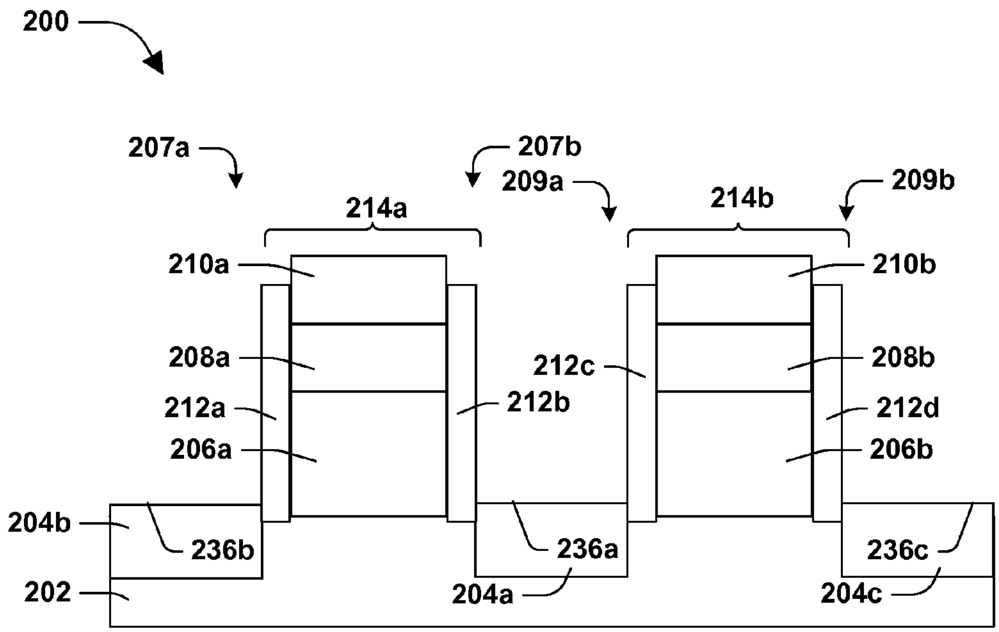

100
Form first alignment spacer 218a on second side 207b of first dummy gate structure 214a and form second alignment spacer 218b on first side 209a of second dummy gate 214b
102
Form first inter layer dielectric (ILD) layer 222 over first active area 204a
104
Form first gate structure 226a in place of first dummy gate structure 214a and form second gate structure 226b in place of second dummy gate structure 214b
106
Remove first ILD layer 222 from over first active area 204a by selective etch
108
Form contact 232 between first alignment spacer 218a and second alignment spacer 218b and in contact with first active area 204a
110

FIG. 1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214b
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210b
208a
208b
212a
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212c
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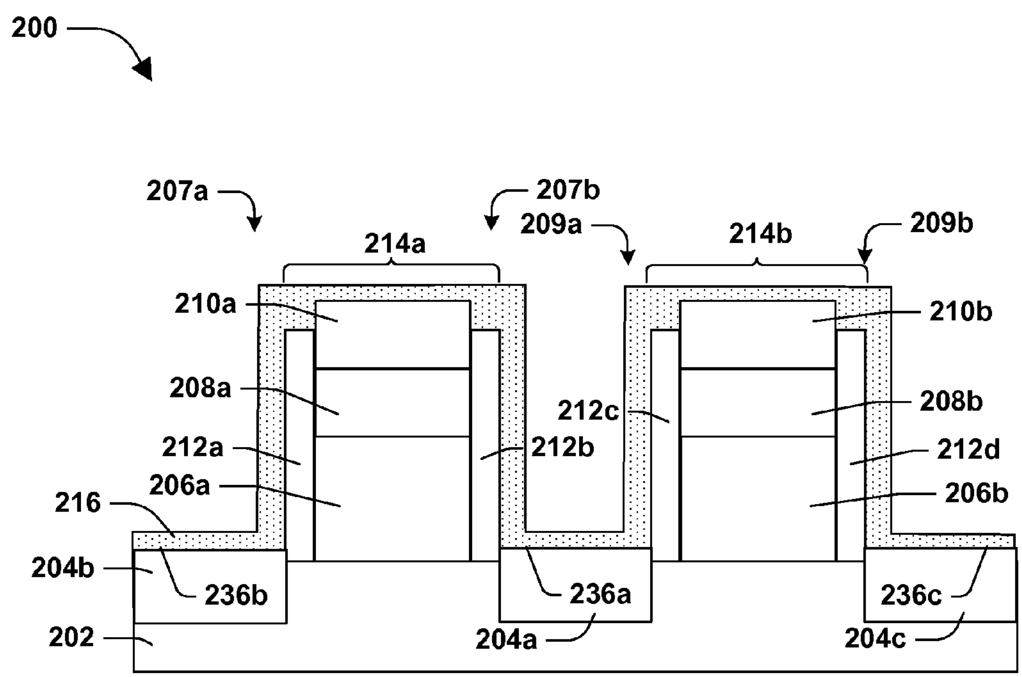
236c
202
204a
204c

FIG. 2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204b
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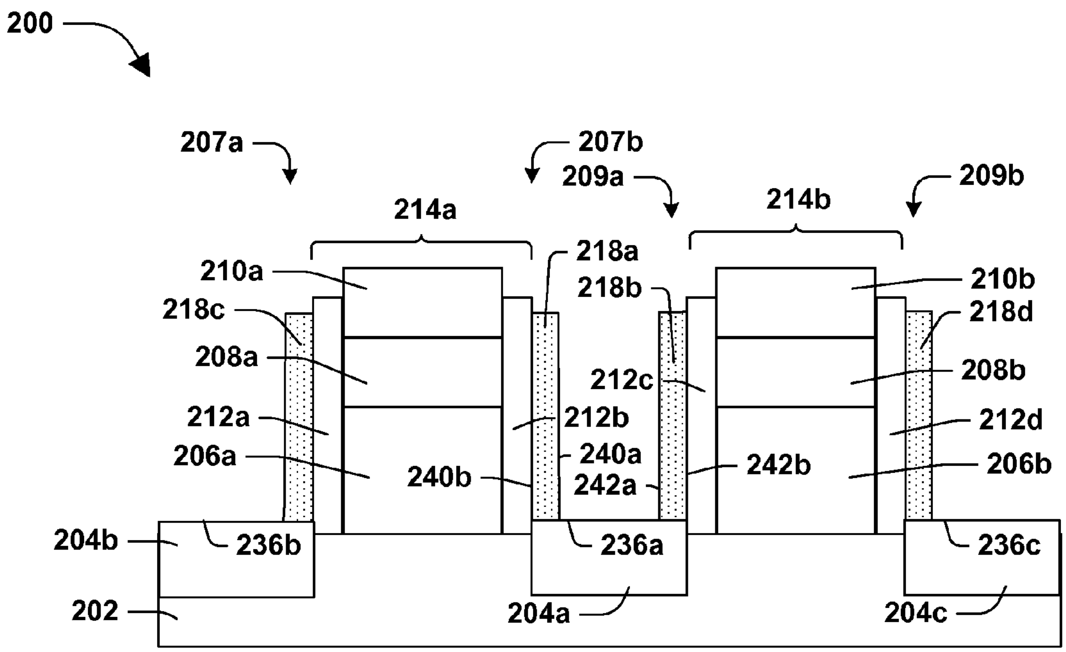
236c
202
204a
204c

FIG. 3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210b
218a
218b
218c
218d
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208b
212a
212b
212c
212d
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242b
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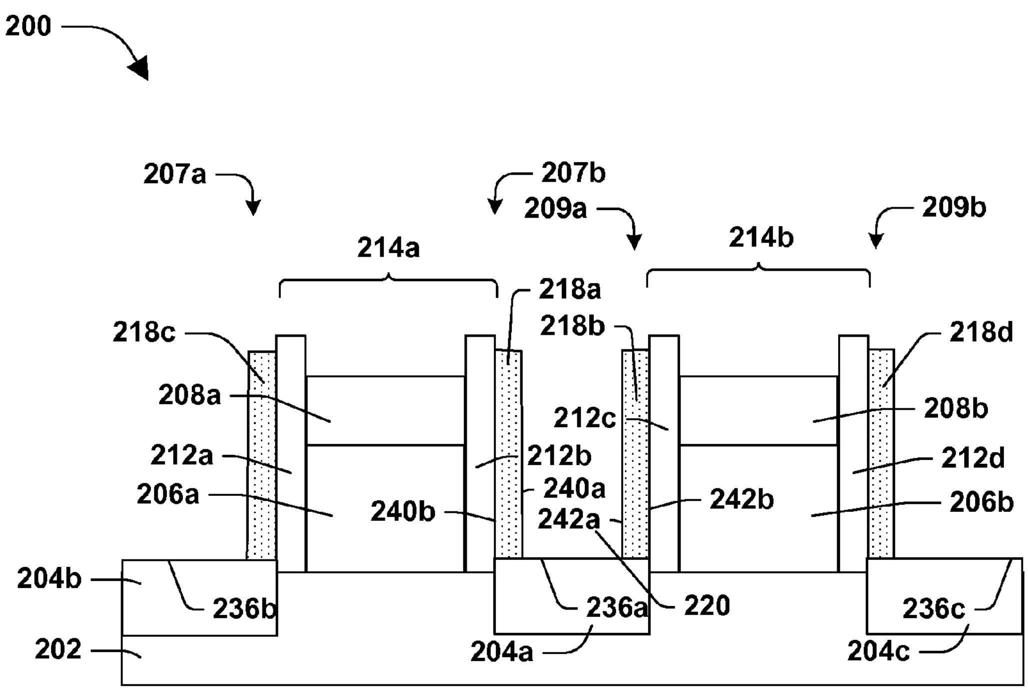
204b
204c
236a
236b
236c
202

FIG. 4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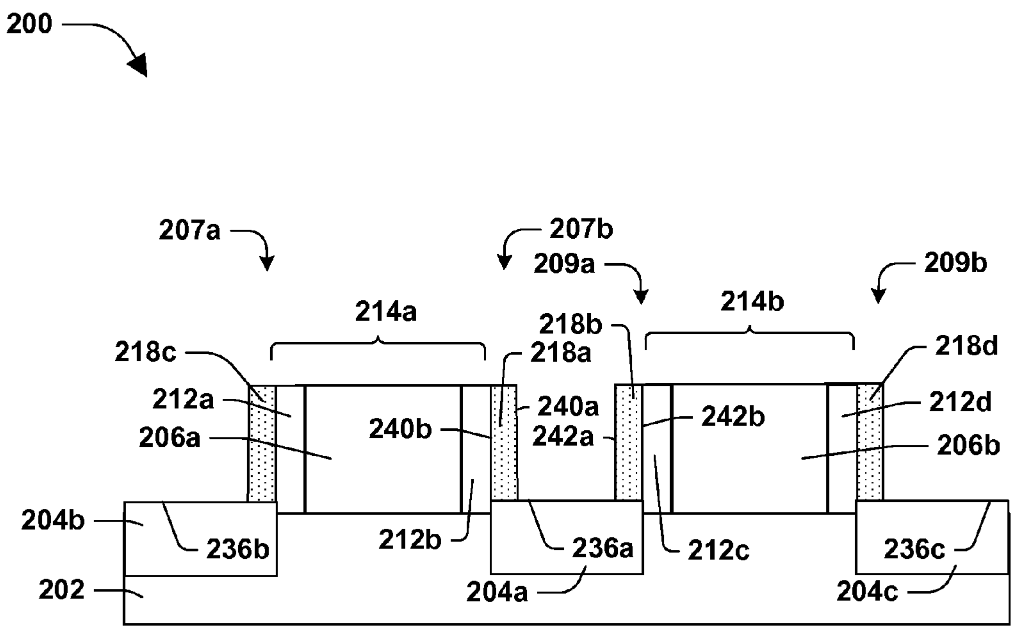
209b
214a
214b
218a
218b
218c
218d
208a
208b
212a
212b
212c
212d
206a
206b
240a
240b
242a
242b
220
204a
204b
204c
236a
236b
236c
202

FIG. 5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209a
209b
214a
214b
218c
218b
218a
218d
212a
240a
212d
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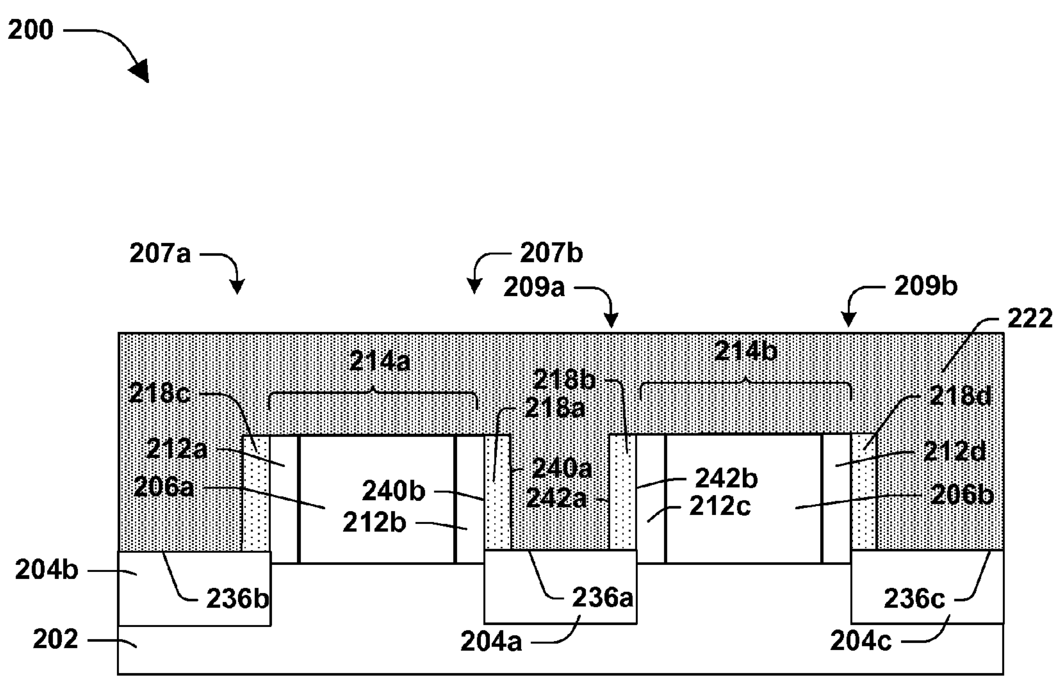
240b
242a
242b
206b
204b
236b
212b
236a
212c
236c
202
204a
204c

FIG. 6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207b
209a
209b
222
214a
214b
218c
218b
218a
218d
212a
240a
212d
206a
240b
242b
242a
212c
206b
212b
204b
236b
236a
236c
202
204a
204c

FIG. 7

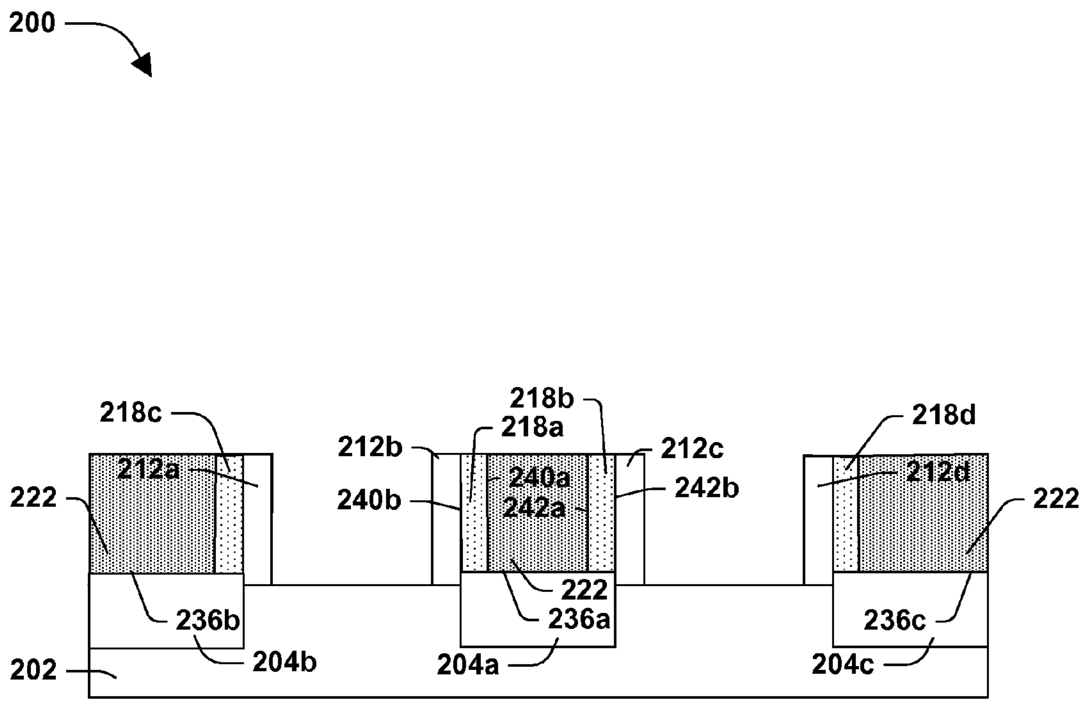
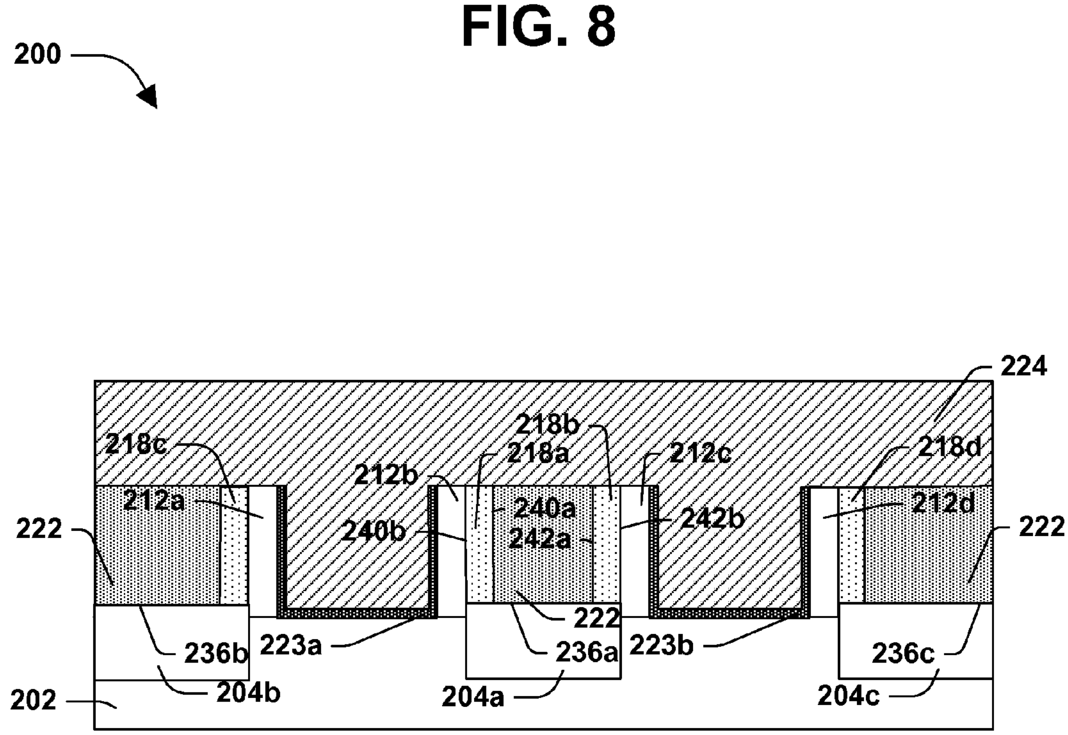

200
218c
212a
222
218b
218a
212b
212c
240a
240b
242a
242b
218d
212d
222
222
236b
236a
236c
202
204b
204a
204c

FIG. 8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218c
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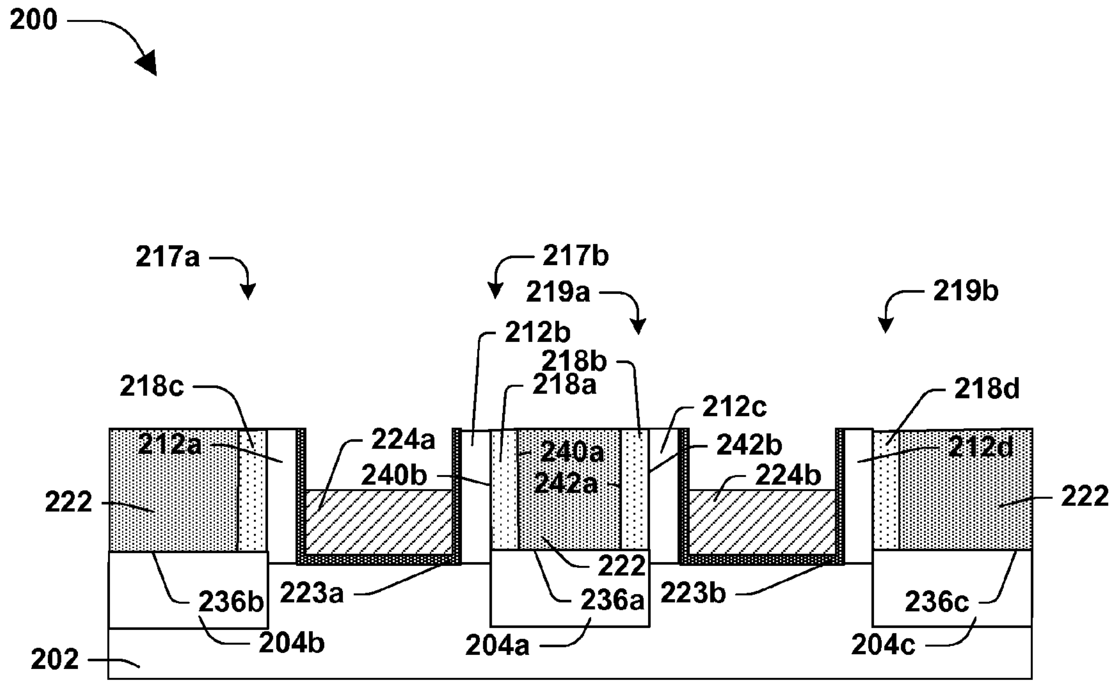
218d
212b
212a
240a
212d
240b
242b
222
242a
222
222
236b
223a
236a
223b
236c
202
204b
204a
204c

FIG. 9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218b
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212c
218c
218d
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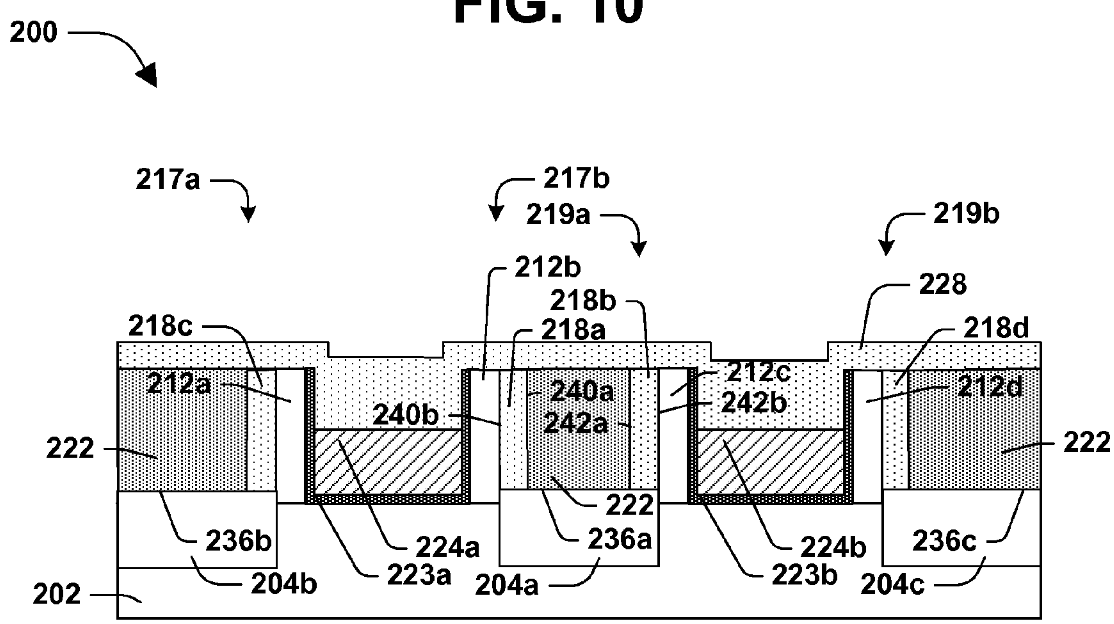
224a
242b
212d
240a
240b
224b
242a
222
222
222
223a
236a
223b
236b
236c
204b
204a
204c
202

FIG. 10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212b
228
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218a
218d
212c
212a
240a
212d
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242b
242a
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224a
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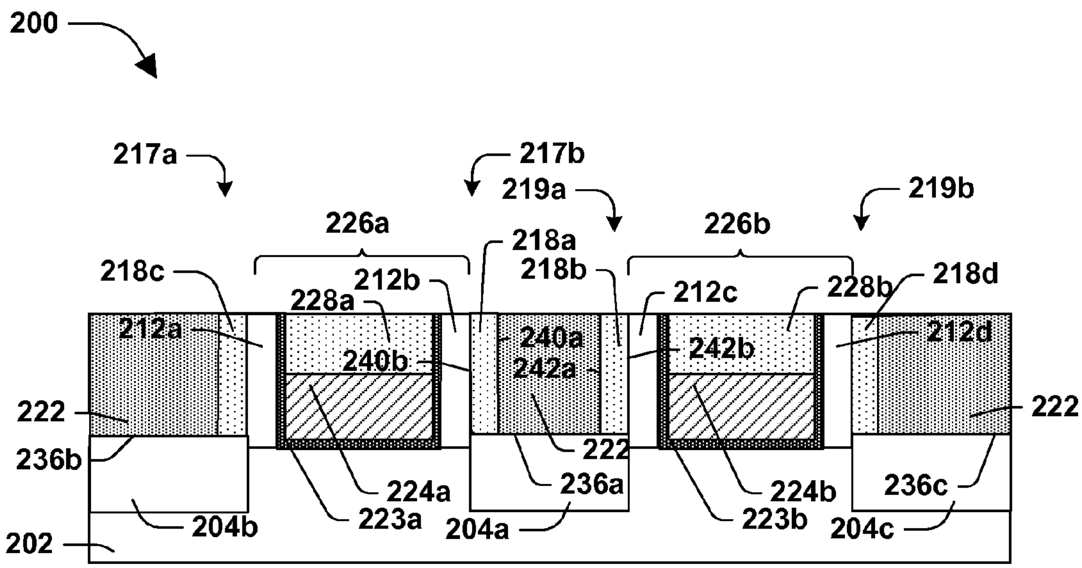
236c
223a
223b
204b
204a
204c
202

FIG. 11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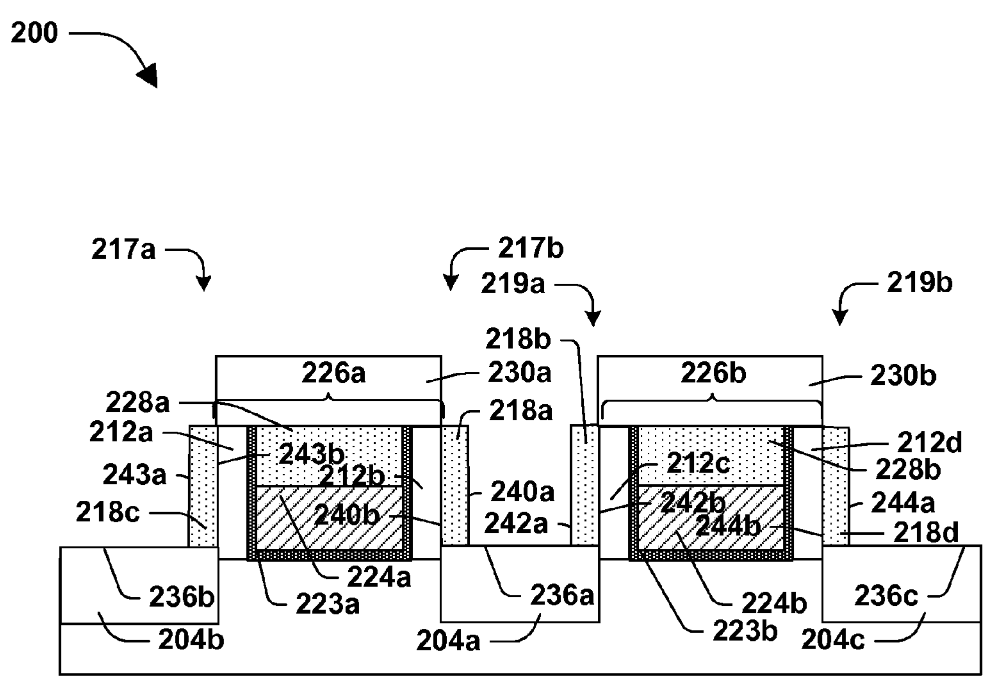
228b
240a
240b
242a
242b
222
222
222
236a
236b
236c
224a
224b
223a
223b
204a
204b
204c
202

FIG. 12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212b
240a
212c
244a
218c
240b
242a
242b
244b
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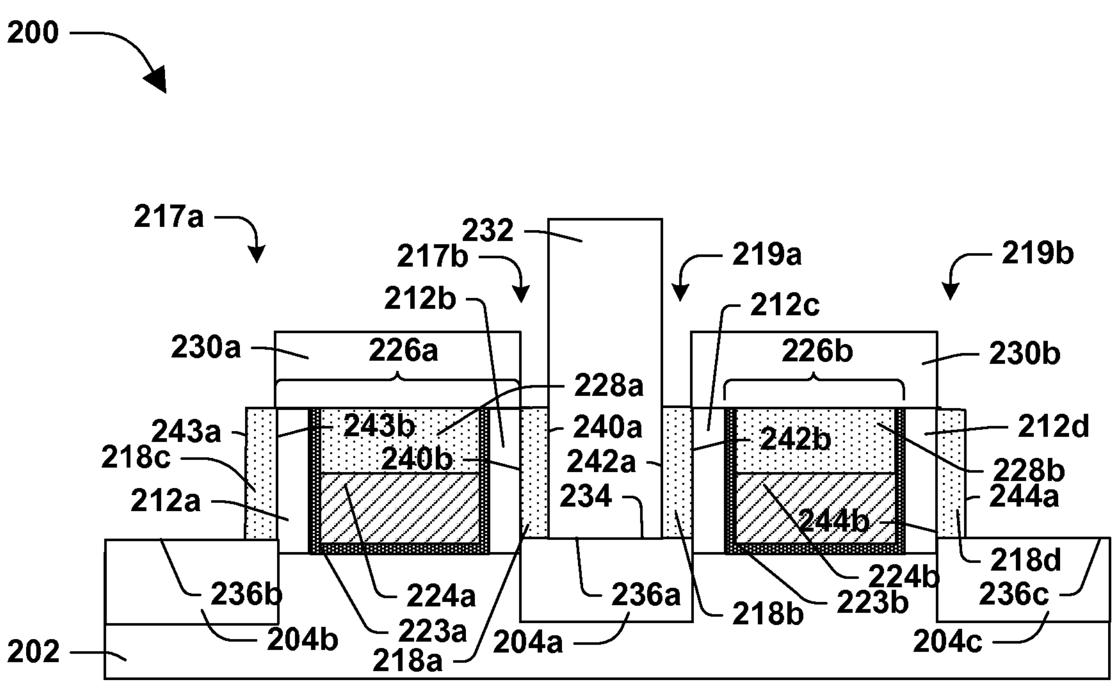
236b
236a
236c
223a
224b
223b
204b
204a
204c

FIG. 13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232
217b
219a
219b
212b
212c
230a
226a
226b
230b
228a
243a
243b
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212d
218c
240b
242a
228b
212a
234
244a
244b
224b
218d
236b
224a
236a
218b
223b
236c
204b
223a
204a
204c
202
218a

FIG. 14

SEMICONDUCTOR ARRANGEMENT AND FORMATION THEREOF

BACKGROUND

Contacts are used to make electrical connections in or among different features in a semiconductor device. A contact, for example, is used to connect one metal layer to another metal layer or another device layer, where the metal layers are otherwise electrically isolated from one another, such as by an insulating or dielectric material separating the metal layers.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flow diagram illustrating a method of forming a semiconductor arrangement, in accordance with some embodiments.

FIG. **2** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **3** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **4** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **5** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **6** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **7** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **8** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **9** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **10** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **11** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **12** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **13** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

FIG. **14** is an illustration of a semiconductor arrangement, in accordance with some embodiments.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for

the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

One or more techniques for forming a semiconductor arrangement and resulting structures formed thereby are provided herein.

A method **100** of forming a semiconductor arrangement **200** according to some embodiments is illustrated in FIG. **1** and one or more structures formed thereby at various stages of fabrication are illustrated in FIGS. **2-14**. According to some embodiments, such as illustrated in FIG. **14**, the semiconductor arrangement **200** comprises a first alignment spacer **218*a*** having a substantially vertical first outer surface **240*a*** on a second side **217*b*** of a first gate structure **226*a***, where the first outer surface **240*a*** is opposite a first inner surface **240*b*** of the first alignment spacer **218*a***. In some embodiments, the first inner surface **240*b*** is in contact with the first gate structure **226*a***. In some embodiments, a second alignment spacer **218*b*** having a substantially vertical second outer surface **242*a*** is on a first side **219*a*** of a second gate structure **226*b***, where the second outer surface **242*a*** is opposite a second inner surface **242*b*** of the second alignment spacer **218*b***. In some embodiments, the second inner surface **242*b*** is in contact with the second gate structure **226*b***. In some embodiments, a conductive contact **232** is in contact with a substantially planar first top surface **236*a*** of a first active area **204*a*** between the first alignment spacer **218*a*** and the second alignment spacer **218*b***. In some embodiments, the conductive contact **232** formed between the first alignment spacer **218*a*** having the substantially vertical first outer surface **240*a*** and the second alignment spacer **218*b*** having the substantially vertical second outer surface **242*a*** has a more desired contact shape then a contact formed between alignments spacers that do not have substantially vertical outer surfaces. In some embodiments, the substantially planar first top surface **236*a*** of the first active area **204*a*** is indicative of a substantially undamaged structure of the first active area **204*a*** as compared to an active area that is not substantially planar. In some embodiments, the substantially undamaged first active area **204*a*** has a greater contact area for the conductive contact **232**, as compared to a damaged first active area. In some embodiments, at least one of the larger contact area of the first active area **204*a*** or the substantially undamaged first active area **204*a*** results in a lower contact resistance between the first active area **204*a*** and the conductive contact **232** as compared to an active area that does not have a larger contact area or is not substantially undamaged. In some embodiments, substantially undamaged is indicative of a substantially uniform lattice structure, such as a lattice structure that has been substantially unaffected by semiconductor processing activities.

At **102** in FIG. **1**, the first alignments spacer **218*a*** is formed on a second side **207*b*** of a first dummy gate structure **214*a*** and the second alignment spacer **218*b*** is formed on a first side **209*a*** of a second dummy gate structure **214*b***, as illustrated in FIG. **4**, according to some embodiments. Turning to FIG. **2**, prior to FIG. **4**, the semiconductor arrangement **200** comprises a substrate **202**, according to some embodiments. In some embodiments, the substrate **202** comprises at least one of silicon or germanium. According to some embodiments, the substrate **202** comprises at least one of an epitaxial layer, a silicon-on-insulator (SOI) structure, a wafer, or a die formed from a wafer. In some embodiments, a first dummy poly **206***a* is on the substrate **202**, an initial first hard mask **208***a* is over the first dummy poly **206***a*, and a first oxide mask **210***a* is over the initial first hard mask **208***a*. In some embodiments, the first dummy gate structure **214***a* comprises a first sidewall spacer **212***a* on a first side **207***a* of the first dummy poly **206***a*, the initial first hard mask **208***a* and the first oxide mask **210***a*, a second sidewall spacer **212***b* on the second side **207***b* of the first dummy poly **206***a*, the initial first hard mask **208***a* and the first oxide mask **210***a* and the first dummy poly **206***a*, the initial first hard mask **208***a* and the first oxide mask **210***a*. In some embodiments, a second dummy poly **206***b* is adjacent the first gate structure **214***a*. In some embodiments, an initial second hard mask **208***b* is over the second dummy poly **206***b*, and a second oxide mask **210***b* is over the initial second hard mask **208***b*. In some embodiments, the second dummy gate structure **214***b* comprises a third sidewall spacer **212***c* on the first side **209***a* of the second dummy poly **206***b*, the initial second hard mask **208***b* and the second oxide mask **210***b*, a fourth sidewall spacer **212***d* on a second side **209***b* of the second dummy poly **206***b*, the initial second hard mask **208***b* and the second oxide mask **210***b* and the second dummy poly **206***b*, the initial second hard mask **208***b* and the second oxide mask **210***b*. In some embodiments, at least one of the first dummy poly **206***a* or the second dummy poly **206***b* comprises an inactive and non-functional material. In some embodiments, the sidewall spacers **212** comprise at least one of silicon, oxide, or nitride. In some embodiments, at least one of the initial first hard mask **208***a* or the initial second hard mask **208***b* comprises at least one of silicon, oxygen, carbon, or nitrogen. In some embodiments, at least one of the first oxide mask **210***a* or the second oxide mask **210***b* comprises oxide. In some embodiments, the first active area **204***a* is between the first dummy gate structure **214***a* and the second dummy gate structure **214***b*. In some embodiments, a second active area **204***b* is on the first side **207***a* of the first dummy gate structure **214***a*. In some embodiments, a third active area **204***c* is on the second side **209***b* of the second dummy gate structure **214***b*. In some embodiments, at least one of the first active area **204***a*, the second active area **204***b*, or the third active area **204***c* comprises an epitaxial (Epi) cap. In some embodiments, the Epi caps are formed over fins formed from the substrate **202**. In some embodiments, the Epi caps are grown, such that the Epi caps are formed over silicon, such as the silicon in the fins. In some embodiments, at least one of the first active area **204***a*, the second active area **204***b*, or the third active area **204***b* comprises at least one of silicon or germanium. In some embodiments, at least one of a first active area **204***a*, the second active area **204***b*, or the third active area **204***b* comprise at least one of a source or a drain.

Turning to FIG. **3**, a layer of alignment material **216** is formed, such as deposited, over the first active area **204***a*, the first dummy gate structure **214***a*, the second active area **204***b*, the second dummy gate structure **214***b*, and the third active area **204***c*, according to some embodiments. In some embodiments, the layer of alignment material **216** has an alignment material width between about 50 nm to about 120 nm. In some embodiments, the layer of alignment material **216** comprises at least one of Si_3N_4, SiON, SiCN or SiOCN. In some embodiments, such as when the layer of alignment material **216** comprises Si_3N_4, the layer of alignment material **216** is formed by deposition in a furnace. In some embodiments, the deposition in the furnace occurs in a furnace chamber. In some embodiments, the deposition in the furnace occurs at a furnace temperature between about 600° C. to about 1400° C. In some embodiments, the deposition in the furnace occurs at a furnace pressure between about 100 mTorr to about 300 mTorr. In some embodiments, the deposition in the furnace occurs while introducing a first furnace gas comprising $SiCl_2H_2$ into the furnace chamber at a first furnace flow rate between about 20 sccm to about 60 sccm. In some embodiments, the deposition in the furnace occurs while introducing a second furnace gas comprising NH_3 into the furnace chamber at a second furnace flow rate between about 200 sccm to about 300 sccm. In some embodiments, such as when the layer of alignment material **216** comprises at least one of Si_3N_4, SiON, SiCN or SiOCN, the layer of alignment material **216** is formed by chemical vapor deposition (CVD). In some embodiments, the CVD occurs in a CVD chamber. In some embodiments, the CVD occurs at a CVD temperature between about 200° C. to about 400° C. In some embodiments, the CVD occurs at a CVD pressure between about 100 mTorr to about 1000 mTorr. In some embodiments, the CVD occurs while introducing a first CVD gas into the CVD chamber comprising at least one of SiH_4 or $SiCl_2H_2$ at a first CVD flow rate between about 500 sccm to about 2000 sccm. In some embodiments, the CVD occurs while introducing a second CVD gas comprising N_2O into the CVD chamber at a second CVD flow rate between about 500 sccm to about 2000 sccm. In some embodiments, the CVD occurs while introducing a third CVD gas comprising at least one of CO_2 of O_2 into the CVD chamber at a third CVD flow rate between about 100 sccm to about 200 sccm. In some embodiments, the CVD occurs where a CVD plasma power is between about 500 W to about 1000 W. In some embodiments, such as when the layer of alignment material **216** comprises at least one of Si_3N_4, SiON, SiCN or SiOCN, the layer of alignment material **216** is formed by atomic layer deposition (ALD). In some embodiments, the ALD occurs in an ALD chamber. In some embodiments, the ALD occurs at an ALD temperature between about 200° C. to about 400° C. In some embodiments, the ALD occurs at an ALD pressure between about 100 mTorr to about 1000 mTorr. In some embodiments, the ALD occurs while introducing a first ALD gas comprising at least one of SiH_4, Si_xC_y, or NH_3 into the ALD chamber at a first ALD flow rate between about 300 sccm to about 800 sccm. In some embodiments, the ALD occurs while introducing a second ALD gas comprising O_2 into the ALD chamber at a second ALD flow rate between about 100 sccm to about 200 sccm. In some embodiments, the ALD occurs where an ALD plasma power is between about 100 W to about 400 W. In some embodiments, a first silicide layer (not shown) is formed over a first top surface **236***a* of the first active area **204***a*, a second silicide layer (not shown) is formed over a second top surface **236***b* of the second active area **204***b*, and a third silicide layer (not shown) is formed over a third top surface **236***c* of the third active area **204***c*. In some embodiments, at least one of the first silicide layer, the second silicide layer or the third silicide layer is formed during at least one of the ALD, CVD or deposition in a furnace.

Turning to FIG. **4**, the layer of alignment material **216** is removed from the first top surface **236***a* of the first active area **204***a*, the second top surface **236***b* of the second active area **204***b*, the third top surface **236***c* of the third active area **204***c*, a top portion of the first dummy gate structure **214***a* and a top portion of the second dummy gate structure **214***b*, according to some embodiments. In some embodiments, the layer of alignment material **216** is removed by a first etch, where the etchant is selective for the layer of alignment material **216**, such that the etchant removes little to none of the first active area **204***a*, the second active area **204***b* or the third active area **204***c*. In some embodiments, the first etch leaves the first top surface **236***a*, the second top surface **236***b*, and the third top surface **236***c* substantially planar. In some embodiments, the removal of the layer of alignment material **216** forms the first alignment spacer **218***a* on the second side **207***b* of the first dummy gate structure **214***a*, the second alignment spacer **218***b* on the first side **209***a* of the second dummy gate structure **214***b*, a third alignment spacer **218***c* on the first side **207***a* of the first dummy gate structure **214***a* and a fourth alignment spacer **218***d* on the second side **209***b* of the second dummy gate structure **214***b*. In some embodiments, the first alignment spacer **218***a* has the substantially vertical first outer surface **240***a* on the second side **207***b* of the first dummy gate structure **214***a*, where the first outer surface **240***a* is opposite the first inner surface **240***b* of the first alignment spacer **218***a*. In some embodiments, the first inner surface **240***b* is in contact with the first dummy gate structure **214***a*. In some embodiments, the second alignment spacer **218***b* has the substantially vertical second outer surface **242***a* on the first side **209***a* of the second dummy gate structure **214***b*, where the second outer surface **242***a* is opposite the second inner surface **242***b* of the second alignment spacer **218***b*. In some embodiments, the second inner surface **242***b* is in contact with the second dummy gate structure **214***b*. In some embodiments, the first alignment spacer **218***a* has a first alignment width between about 50 nm to about 120 nm. In some embodiments, the second alignment spacer **218***b* has a second alignment width between about 50 nm to about 120 nm. In some embodiments, the third alignment spacer **218***c* has a third alignment width between about 50 nm to about 120 nm. In some embodiments, the fourth alignment spacer **218***d* has a fourth alignment width between about 50 nm to about 120 nm.

Turning to FIG. **5**, the first oxide mask **210***a* and the second oxide mask **210***b* are removed, such as by etching, according to some embodiments. In some embodiments, the initial first hard mask **208***a*, a portion of the first sidewall spacer **212***a* and a portion of the second sidewall spacer **212***b* above the first dummy poly **206***a*, a portion of the first alignment spacer **218***a* and a portion of the third alignment spacer **218***c* above the first dummy poly **206***a* are removed, such as by chemical mechanical planarization (CMP), as illustrated in FIG. **6**. In some embodiments, the initial second hard mask **208***b*, a portion of the third sidewall spacer **212***c* and a portion of the fourth sidewall spacer **212***d* above the second dummy poly **206***b*, and a portion of the second alignment spacer **218***b* and a portion of the fourth alignment spacer **218***d* above the second dummy poly **206***b* are removed, such as by CMP. In some embodiments, the CMP exposes a top surface of the first dummy poly **206***a* and a top surface of the second dummy poly **206***b*. In some embodiments, the top surface of the first dummy poly **206***a* and the top surface of the second dummy poly **206***b* lie in a first plane. In some embodiments, top surfaces of the third alignment spacer **218***c*, the first sidewall spacer **212***a*, the second sidewall spacer **212***b*, the first alignment spacer **218***a*, the second alignment spacer **218***b*, the third sidewall spacer **212***c*, the fourth sidewall spacer **212***d*, and the fourth alignment spacer **218***d* lie in the first plane.

At **104** in FIG. **1**, a first inter layer dielectric (ILD) layer **222** is formed over the first active area **204***a*, as illustrated in FIG. **7**, according to some embodiments. In some embodiments, the ILD layer **222** is formed over the second active area **204***b*, the third alignment spacer **218***c*, the first dummy gate structure **214***a*, the first alignment spacer **218***a*, the second alignment spacer **218***b*, the second dummy gate **214***b*, the fourth alignment spacer **218***d* and the third active area **204***b*. In some embodiments, the ILD layer **222** is formed by deposition. In some embodiments, the ILD layer **222** comprises at least one of oxide or nitride. In some embodiments, a top portion of the ILD layer **222** is removed, such that the top surface of the third alignment spacer **218***c*, the first sidewall spacer **212***a*, the dummy poly **206***a*, the second sidewall spacer **212***b*, the first alignment spacer **218***a*, the second alignment spacer **218***b*, the second dummy poly **206***b*, the third sidewall spacer **212***c*, the fourth sidewall spacer **212***d*, and the fourth alignment spacer **218***d* are exposed, as illustrated in FIG. **8**. In some embodiments, the top portion of the ILD layer **222** is removed by CMP.

With continued reference to FIG. **8**, the first dummy poly **206***a* and the second dummy poly **206***b* are removed, according to some embodiments. In some embodiments, the first dummy poly **206***a* and the second dummy poly **206***b* are removed by etching. In some embodiments, the removal of the first dummy poly **206***a* and the second dummy poly **206***b* exposes a top surface of the substrate **202** between the first sidewall spacer **212***a* and the second sidewall spacer **212***b* and exposes a top surface of the substrate **202** between the third sidewall spacer **212***c* and the fourth sidewall spacer **212***d*.

At **106** in FIG. **1**, the first gate structure **226***a* is formed in place of the first dummy gate structure **214***a* and the second gate structure **226***b* is formed in place of the second dummy gate structure **214***b*, as illustrated in FIG. **12**, according to some embodiments. Turning to FIG. **9**, prior to FIG. **12**, a first glue layer **223***a* is formed over the top surface of the substrate **202** between the first sidewall spacer **212***a* and the second sidewall spacer **212***b*, on a sidewall of the first sidewall spacer **212***a* and on a sidewall of the second sidewall spacer **212***b*. In some embodiments, a second glue layer **223***b* is formed over the top surface of the substrate **202** between the third sidewall spacer **212***c* and the fourth sidewall spacer **212***d*, on a sidewall of the third sidewall spacer **212***c* and on a sidewall of the fourth sidewall spacer **212***d*. In some embodiments, the first glue layer **223***a* and the second glue layer **223***b* comprise at least one of titanium or nitride. In some embodiments, at least one of the first glue layer **223***a* or the second glue layer **223***b* have a thickness between about 30 Å to about 150 Å. In some embodiments, a layer of gate electrode material **224** is formed over the ILD layer **222**, the sidewall spacers **212**, the alignment spacers **218**, the first glue layer **223***a* and the second glue layer **223***b*. In some embodiments, the layer of gate electrode material **224** comprises a metal, such as at least one of tungsten, aluminum, titanium or cobalt. In some embodiments, a top portion of the layer of gate electrode material **224** is removed, such as by CMP, to expose the top surface of the third alignment spacer **218***c*, the first sidewall spacer **212***a*, the first glue layer **223***a*, the second sidewall spacer **212***b*, the first alignment spacer **218***a*, the second alignment spacer **218***b*, the third sidewall spacer **212***c*, the second glue layer **223***b*, the fourth sidewall spacer **212***d*, and the fourth alignment spacer **218***d*, as illustrated in FIG. **10**.

With continued reference to FIG. **10**, a first height of the layer of gate material **224** over the first glue layer **223***a* is reduced, such that a top surface of the layer of gate material is below the top surface of the first glue layer **223***a*, forming the first gate electrode **224***a*, according to some embodiments. In some embodiments, a second height of the layer of gate material **224** over the second glue layer **223***b* is reduced, such that a top surface of the layer of gate material **224** is below the top surface of the second glue layer **223***b*, forming the second gate electrode **224***b*.

Turning to FIG. **11**, a layer of hard mask material **228** is formed over the ILD layer **222**, the third alignment spacer **218***c*, the first sidewall spacer **212***a*, the first glue layer **223***a*, the first gate electrode **224***a* the second sidewall spacer **212***b*, the first alignment spacer **218***a*, the second alignment spacer **218***b*, the third sidewall spacer **212***c* the second glue layer **223***b*, the second gate electrode **224***b*, the fourth sidewall spacer **212***d*, and the fourth alignment spacer **218***d*. In some embodiments, the layer of hard mask material **228** is formed by deposition. In some embodiments, the layer of hard mask material **228** comprises at least one of Si_3N_4, SiON, SiCN or SiOCN.

Turning to FIG. **12**, a top portion of the layer of hard mask material **228** is removed, such as by CMP, forming a first hard mask **228***a* over the first gate electrode **224***a* and forming a second hard mask **228***b* over the second gate electrode **224***b*. In some embodiments, the first gate structure **226***a* comprises the first sidewall spacer **212***a*, the first glue layer **223***a*, the first gate electrode **224***a*, the first hard mask **228***a* and the second sidewall spacer **212***b*. In some embodiments, the second gate structure **226***b* comprises the third sidewall spacer **212***c*, the second glue layer **223***b*, the second gate electrode **224***b*, the second hard mask **228***b* and the fourth sidewall spacer **212***d*. In some embodiments, the removal of the top portion of the layer of hard mask material **228** exposes top surfaces of the ILD layer **222**, the third alignment spacer **218***c*, the first sidewall spacer **212***a*, the first glue layer **223***a*, the second sidewall spacer **212***b*, the first alignment spacer **218***a*, the second alignment spacer **218***b*, the third sidewall spacer **212***c*, the second glue layer **223***b*, the fourth sidewall spacer **212***d*, and the fourth alignment spacer **218***d*, according to some embodiments.

Turning to FIG. **13**, a first ILD cap **230***a* is formed over the first gate structure **226***a* and a second ILD cap **230***b* is formed over the second gate structure **226***b*, according to some embodiments. In some embodiments, at least one of the first ILD cap **230***a* or the second ILD cap **230***b* is formed by deposition. In some embodiments, at least one of the first ILD cap **230***a* or the second ILD cap **230***b* comprises at least one of nitride or oxide.

At **108** in FIG. **1**, the ILD layer **222** is removed from over the first active area **204***a* by a selective etch, as illustrated in FIG. **13**, according to some embodiments. In some embodiments, the ILD layer **222** is removed from over the second active area **204***b* and the third active area **204***c* by selective etch. In some embodiments, the selective etch causes little to no damage to at least one of the first active area **204***a*, the second active area **204***b*, or the third active area **204***c*. In some embodiments, after the selective etch the first alignment spacer **218***a* has a substantially vertical first outer surface **240***a* on the second side **217***b* of the first gate structure **226***a*, where the first outer surface **240***a* is opposite the first inner surface **240***b* of the first alignment spacer **218***a*. In some embodiments, after the selective etch the second alignment spacer **218***b* has a substantially vertical second outer surface **242***a* on the first side **219***a* of the second gate structure **226***b*, where the second outer surface **242***a* is opposite the second inner surface **242***b* of the second alignment spacer **218***b*. In some embodiments, after the selective etch the third alignment spacer **218***c* has a substantially vertical third outer surface **243***a* on a first side **217***a* of the first gate structure **226***a*, where the third outer surface **243***a* is opposite a third inner surface **243***b* of the third alignment spacer **218***c*. In some embodiments, the third inner surface **243***b* is in contact with the first gate structure **226***a*. In some embodiments, after the selective etch the fourth alignment spacer **218***d* has a substantially vertical fourth outer surface **244***a* on a second side **219***b* of the second gate structure **226***b*, where the fourth outer surface **244***a* is opposite the fourth inner surface **244***b* of the fourth alignment spacer **218***d*. In some embodiments, the fourth inner surface **244***b* is in contact with the second gate structure **226***b*.

At **110** in FIG. **1**, the conductive contact **232** is formed between the first alignment spacer **218***a* and the second alignment spacer **218***b*, such that the conductive contact **232** is in contact with the first top surface **236***a* of the first active area **204***a*, as illustrated in FIG. **14**. In some embodiments, the conductive contact **232** comprises metal. In some embodiments, the first alignment spacer **218***a* and the second alignment spacer **218***b* align the conductive contact **232** such that the conductive contact **232** is formed over and in contact with the first active area **204***a*. In some embodiments, the conductive contact **232** formed between the first alignment spacer **218***a* having the substantially vertical first outer surface **240***a* and the second alignment spacer **218***b* having the substantially vertical second outer surface **242***a* has a more desired contact shape then a contact formed between alignments spacers that do not have substantially vertical outer surfaces. In some embodiments, the substantially planar first top surface **236***a* of the first active area **204***a* is indicative of a substantially undamaged structure of the first active area **204***a* as compared to an active area that is not substantially planar. In some embodiments, the substantially undamaged first active area **204***a* has a greater contact area for the conductive contact **232**, as compared to a damaged first active area. In some embodiments, at least one of the larger contact area of the first active area **204***a* or the substantially undamaged first active area **204***a* results in a lower contact resistance between the first active area **204***a* and the conductive contact **232** as compared to an active area that does not have a larger contact area or is not substantially undamaged. In some embodiments, substantially undamaged is indicative of a substantially uniform lattice structure, such as a lattice structure that has been substantially unaffected by semiconductor processing activities.

According to some embodiments, a semiconductor arrangement comprises a first alignment spacer having a substantially vertical first outer surface on a second side of a first gate structure, where the first outer surface is opposite a first inner surface of the first alignment spacer. In some embodiments, the first inner surface is in contact with the first gate structure. In some embodiments, a second alignment spacer having a substantially vertical second outer surface is on a first side of a second gate structure, where the second outer surface is opposite a second inner surface of the second alignment spacer. In some embodiments, the second inner surface is in contact with the second gate structure. In some embodiments, a conductive contact in contact with a substantially planar surface of a first active area is between the first alignment spacer and the second alignment spacer.

According to some embodiments, a method of forming a semiconductor arrangement comprises forming a first alignment spacer on a second side of a first dummy gate structure and forming a second alignment spacer on a first side of a second dummy gate structure, such that a first active area is between the first alignment spacer and the second alignment spacer. According to some embodiments, the method of forming a semiconductor arrangement further comprises forming a first inter layer dielectric (ILD) layer over the first active area, forming a first gate structure in place of the first dummy gate structure, and forming a second gate structure in place of the second dummy gate structure. According to some embodiments, the method of forming a semiconductor arrangement further comprises removing the first ILD layer from over the first active area by selective etch, such that the first active area has a substantially planar surface.

According to some embodiments, a semiconductor arrangement comprises a first alignment spacer having a substantially vertical first outer surface on a second side of a first gate structure, where the first outer surface is opposite a first inner surface, the first inner surface in contact with the first gate structure and a second alignment spacer having a substantially vertical second outer surface is on a first side of a second gate structure where the second outer surface is opposite a second inner surface, the second inner surface in contact with the second gate structure. In some embodiments, a third alignment spacer having a substantially vertical third outer surface is on a first side of the first gate structure, where the third outer surface is opposite a third inner surface, the third inner surface in contact with the first gate structure. In some embodiments, a fourth alignment spacer having a substantially vertical fourth outer surface is on a second side of the second gate structure where the fourth outer surface is opposite a fourth inner surface, the fourth inner surface in contact with the second gate structure. In some embodiments, a contact is in contact with a first active area between the first alignment spacer and the second alignment spacer, where the first active area has little to no surface damage.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Various operations of embodiments are provided herein. The order in which some or all of the operations are described should not be construed to imply that these operations are necessarily order dependent. Alternative ordering will be appreciated having the benefit of this description. Further, it will be understood that not all operations are necessarily present in each embodiment provided herein. Also, it will be understood that not all operations are necessary in some embodiments.

It will be appreciated that layers, features, elements, etc. depicted herein are illustrated with particular dimensions relative to one another, such as structural dimensions or orientations, for example, for purposes of simplicity and ease of understanding and that actual dimensions of the same differ substantially from that illustrated herein, in some embodiments. Additionally, a variety of techniques exist for forming the layers features, elements, etc. mentioned herein, such as etching techniques, implanting techniques, doping techniques, spin-on techniques, sputtering techniques such as magnetron or ion beam sputtering, growth techniques, such as thermal growth or deposition techniques such as chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced chemical vapor deposition (PECVD), or atomic layer deposition (ALD), for example.

Moreover, "exemplary" is used herein to mean serving as an example, instance, illustration, etc., and not necessarily as advantageous. As used in this application, "or" is intended to mean an inclusive "or" rather than an exclusive "or". In addition, "a" and "an" as used in this application and the appended claims are generally be construed to mean "one or more" unless specified otherwise or clear from context to be directed to a singular form. Also, at least one of A and B and/or the like generally means A or B or both A and B. Furthermore, to the extent that "includes", "having", "has", "with", or variants thereof are used, such terms are intended to be inclusive in a manner similar to the term "comprising". Also, unless specified otherwise, "first," "second," or the like are not intended to imply a temporal aspect, a spatial aspect, an ordering, etc. Rather, such terms are merely used as identifiers, names, etc. for features, elements, items, etc. For example, a first element and a second element generally correspond to element A and element B or two different or two identical elements or the same element.

Also, although the disclosure has been shown and described with respect to one or more implementations, equivalent alterations and modifications will occur to others skilled in the art based upon a reading and understanding of this specification and the annexed drawings. The disclosure comprises all such modifications and alterations and is limited only by the scope of the following claims. In particular regard to the various functions performed by the above described components (e.g., elements, resources, etc.), the terms used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure. In addition, while a particular feature of the disclosure may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application.

What is claimed is:

1. A semiconductor arrangement comprising:

a first gate structure comprising:

a first sidewall spacer;

a second sidewall spacer;

a first glue layer between the first sidewall spacer and the second sidewall spacer;

a first gate electrode over the first glue layer and between the first sidewall spacer and the second sidewall spacer; and

a first hard mask over the first gate electrode and between the first sidewall spacer and the second sidewall spacer;

a first alignment spacer having a substantially vertical first outer surface on a second side of the first gate structure, where the first outer surface is opposite a first inner surface of the first alignment spacer, the first inner surface in contact with the second sidewall spacer of the first gate structure;

a second alignment spacer having a substantially vertical second outer surface on a first side of a second gate structure, where the second outer surface is opposite a second inner surface of the second alignment spacer, the second inner surface in contact with the second gate structure; and

a conductive contact in contact with a substantially planar surface of a first active area between the first alignment spacer and the second alignment spacer.

2. The semiconductor arrangement of claim **1**, the second gate structure comprising:

a third sidewall spacer, the second alignment spacer in contact with third sidewall spacer;

a fourth sidewall spacer;

a second glue layer between the third sidewall spacer and the fourth sidewall spacer;

a second gate electrode over the second glue layer and between the third sidewall spacer and the fourth sidewall spacer; and a second hard mask over the second gate electrode and between the third sidewall spacer and the fourth sidewall spacer.

3. The semiconductor arrangement of claim **2**, at least one of:

the first glue layer between the first sidewall spacer and the first gate electrode;

the first glue layer between the second sidewall spacer and the first gate electrode;

the second glue layer between the third sidewall spacer and the second gate electrode; or

the second glue layer between the fourth sidewall spacer and the second gate electrode.

4. The semiconductor arrangement of claim **1**, comprising a first interlayer dielectric cap over the first gate structure.

5. The semiconductor arrangement of claim **1**, comprising a second interlayer dielectric cap over the second gate structure.

6. The semiconductor arrangement of claim **1**, at least one of:

the first alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN; or

the second alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN.

7. The semiconductor arrangement of claim **1**, comprising:

a third alignment spacer having a substantially vertical third outer surface on a first side of the first gate structure, where the third outer surface is opposite a third inner surface of the third alignment spacer, the third inner surface in contact with the first gate structure; and

a fourth alignment spacer having a substantially vertical fourth outer surface on a second side of the second gate structure, where the fourth outer surface is opposite a fourth inner surface of the fourth alignment spacer, the fourth inner surface in contact with the second gate structure.

8. The semiconductor arrangement of claim **7**, at least one of:

the third alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN; or

the fourth alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN.

9. The semiconductor arrangement of claim **1**, at least one of:

the first alignment spacer having a first alignment width between about 50 nm to about 120 nm; or

the second alignment spacer having a second alignment width between about 50 nm to about 120 nm.

10. A semiconductor arrangement comprising:

a first gate structure comprising:

a first gate electrode over a first glue layer;

a first hard mask over the first gate electrode;

a first sidewall spacer on a first side of the first gate electrode, the first glue layer and the first hard mask; and

a second sidewall spacer on a second side of the first gate electrode, the first glue layer and the first hard mask;

a first alignment spacer having a substantially vertical first outer surface on a second side of the first gate structure, where the first outer surface is opposite a first inner surface, the first inner surface in contact with the first gate structure;

a second alignment spacer having a substantially vertical second outer surface on a first side of a second gate structure where the second outer surface is opposite a second inner surface, the second inner surface in contact with the second gate structure;

a third alignment spacer having a substantially vertical third outer surface on a first side of the first gate structure, where the third outer surface is opposite a third inner surface, the third inner surface in contact with the first gate structure;

a fourth alignment spacer having a substantially vertical fourth outer surface on a second side of the second gate structure where the fourth outer surface is opposite a fourth inner surface, the fourth inner surface in contact with the second gate structure; and

a conductive contact in contact with a first active area between the first alignment spacer and the second alignment spacer, where the first active area has little to no surface damage.

11. The semiconductor arrangement of claim **10**,

the second gate structure comprising:

a second gate electrode over a second glue layer;

a second hard mask over the second gate electrode;

a third sidewall spacer on a first side of the second gate electrode, the second glue layer and the second hard mask; and

a fourth sidewall spacer on a second side of the second gate electrode, the second glue layer and the second hard mask.

12. The semiconductor arrangement of claim **10**,

the first glue layer between the first sidewall spacer and the first gate electrode and the first glue layer between the second sidewall spacer and the first gate electrode.

13. The semiconductor arrangement of claim **10**, at least one of:

a first interlayer dielectric cap over the first gate structure; or

a second interlayer dielectric cap over the second gate structure.

14. The semiconductor arrangement of claim **10**, at least one of:

the first alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN; or

the second alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN.

15. The semiconductor arrangement of claim **10**, at least one of:

the first alignment spacer having a first alignment width between about 50 nm to about 120 nm; or

the second alignment spacer having a second alignment width between about 50 nm to about 120 nm.

16. A semiconductor arrangement comprising:

a source/drain region;

an alignment spacer vertically overlapping the source/drain region;

a gate structure adjacent the alignment spacer and comprising:

a gate electrode over a glue layer;

a hard mask over the gate electrode;

a first sidewall spacer on a first side of the gate electrode and in contact with an inner surface of the alignment spacer, the alignment spacer comprising a first material composition and the first sidewall spacer comprising a second material composition different than the first material composition; and

a second sidewall spacer on a second side of the gate electrode; and

a conductive contact in contact with an outer surface of the alignment spacer and in contact with a top surface of the source/drain region.

17. The semiconductor arrangement of claim **16**, wherein the outer surface of the alignment spacer is substantially planar.

18. The semiconductor arrangement of claim **16**, the alignment spacer comprising at least one of Si_3N_4, SiON, SiCN or SiOCN.

19. The semiconductor arrangement of claim **16**,

the gate electrode laterally co-planar with the first sidewall spacer; and

a top surface of the hard mask laterally co-planar with a top surface of the alignment spacer.

20. The semiconductor arrangement of claim **16**, the top surface of the source/drain region being substantially planar.

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